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**From:** Bruce T. Neel
**Tel:** 602.445.8000
**E-Mail:** NeelT@gtlaw.com

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| Examiner Thao P. LE | ~~703-872-9306~~ 571-273-8300 | USPTO | |

**File No.:** 72145.012400

**Re:** Applicant: Johnson, et al.
Ser. No.: 10/672,165
Filed: September 26, 2003
Title: WAFER-LEVEL MOAT STRUCTURES

**Date:** December 15, 2005 08:41 AM

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**Notes:** Enclosed herewith is the Supplemental Amendment and Response to Final Action Under 37 C.F.R. 1.116

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2375 East Camelback Road, Suite 700, Phoenix, Arizona 85016 Phone: 602.445.8000 Fax: 602.445.8100

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**EXPEDITED PROCEDURE – EXAMINING GROUP 2818**

**PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Applicant: | Johnson et al. | Examiner: | LE, Thao P. |
| Serial No. | 10/672,165 | Group Art Unit: | 2818 |
| Filed: | September 26, 2003 | Docket No. | 72145.012400/US |
| Title: | WAFER-LEVEL MOAT STRUCTURES | | |
| Customer No.: | 33717 | | |

**CERTIFICATE UNDER 37 CFR 1.6(d)**

I hereby certify that this correspondence and identified enclosures are being transmitted via facsimile only to the U.S. Patent and Trademark Office, Central Facsimile No. (571) 273-8300 on December 15, 2005.

Melissa Lusian

**SUPPLEMENTAL AMENDMENT AND RESPONSE TO**

**FINAL ACTION UNDER 37 C.F.R. 1.116**

MAIL STOP AF
Commissioner for Patents
Post Office Box 1450
Alexandria, Virginia 22313-1450

Sir/Madam:

In response to the final Office Action mailed July 12, 2005, and as supplemental to Applicant's prior complete first reply to such Office Action faxed on October 18, 2005, and further in response to and as requested by the Examiner in a telephone interview with Applicant's attorney on November 9, 2005, Applicant submits the following supplemental response.

An extension of time under 37 CFR 1.136 is not necessary when submitting a supplmemental reply to an Office action if a complete first reply was timely filed in reply

to the Office action. Applicant's first reply was timely filed by virtue of the one-month extension of time obtained by Applicant in the first reply.

Kindly enter the following amendments:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 3 of this paper.

**Remarks** begin on page 7 of this paper.

## AMENDMENTS TO THE CLAIMS

**Claim 1 (currently amended)** A chip scale package of an integrated circuit, comprising:

(a) at least one solder ball pad; and

(b) a moat around each solder ball pad for containing liquefied material that flows to the moat, wherein the liquefied material is provided for forming around a solder ball on the solder ball pad.

**Claim 2 (original)** The chip scale package of claim 1, in which at least one passivation layer is disposed on the integrated circuit, and in which the moat is formed in the at least one passivation layer.

**Claim 3 (original)** The chip scale package of claim 2, in which the at least one passivation layer comprises a photo-imageable polymer film.

**Claim 4 (original)** The chip scale package of claim 2, in which the at least one passivation layer has a thickness, and the moat is a full-depth moat having a thickness substantially equal to the thickness of the at least one passivation layer.

**Claim 5 (original)** The chip scale package of claim 4, in which the at least one passivation layer comprises a photo-imageable polymer film.

**Claim 6 (original)** The chip scale package of claim 2, in which the at least one passivation layer has a thickness, and the moat is a partial-depth moat having a thickness of approximately 1-99% of the thickness of the at least one passivation layer.

**Claim 7 (original)** The chip scale package of claim 6, in which the at least one passivation layer comprises a photo-imageable polymer film.

**Claim 8 (original)** The chip scale package of claim 1, in which a first passivation layer is disposed on the integrated circuit, and a second passivation layer, having a thickness, is

disposed on the first passivation layer, and in which the moat is formed in the second passivation layer.

**Claim 9 (original)** The chip scale package of claim 8, in which the moat is a full-depth moat having a moat depth substantially equal to the thickness of the second passivation layer.

**Claim 10 (original)** The chip scale package of claim 9, in which at least the second passivation layer comprises a photo-imageable polymer film.

**Claim 11 (original)** The chip scale package of claim 8, in which the moat is a partial-depth moat having a moat depth of approximately 1-99% the thickness of the second passivation layer.

**Claim 12 (original)** The chip scale package of claim 11, in which at least the second passivation layer comprises a photo-imageable polymer film.

**Claim 13 (original)** A wafer for a chip scale package, the wafer having at least one solder ball pad, comprising:

(a) a solder ball at each solder ball pad;

(b) a polymer collar around the solder ball; and

(c) a moat around each solder ball pad.

**Claim 14 (original)** The wafer of claim 13, such that the moat prevents flow of liquefied polymer collar from within the moat to without the moat during and subsequent to heating of the wafer.

**Claims 15-21 (canceled)**

**Claim 22 (previously presented)** The method of claim 2, in which the at least one passivation layer is an insulating layer.

**Claim 23 (previously presented)** The method of claim 13, in which the moat is positioned relative to the solder ball pad to contain liquefied material that may flow to the moat in a direction substantially away from the solder ball pad.

**Claim 24 (previously presented)** The method of claim 13, in which at least a portion of the polymer collar is positioned at a height, relative to the wafer, above the top of the moat.

**Claim 25 (previously presented)** The method of claim 13, in which the moat is formed in a passivation layer.

**Claim 26 (previously presented)** The method of claim 13, in which the moat is formed in an insulating layer.

**Claim 27 (new)** A chip scale package of an integrated circuit, comprising:

(a) at least one solder ball pad;

(b) a moat around each solder ball pad;

(c) a first passivation layer disposed on the integrated circuit; and

(d) a second passivation layer disposed on the first passivation layer, wherein the moat is formed in the second passivation layer.

**Claim 28 (new)** A chip scale package of an integrated circuit, comprising:

(a) at least one solder ball pad;

(b) a solder ball at each solder ball pad;

(c) a collar around the solder ball; and

(d) a moat around each solder ball pad for containing liquefied material from the collar that flows to the moat.

**Claim 29 (new)** A chip scale package of an integrated circuit disposed in a semiconductor substrate, comprising:

(a) at least one solder ball pad;

(b) a moat around each solder ball pad; and

(c) at least one passivation layer disposed on the integrated circuit, wherein the moat is formed in the at least one passivation layer, but not in the semiconductor substrate.

**Claim 30 (new)** The wafer of claim 14, such that the moat further prevents flow of liquefied polymer collar from within the moat to without the moat prior to heating of the wafer.

**Claim 31 (new)** The chip scale package of claim 1 wherein the liquefied material is provided for forming a collar around the solder ball.

## REMARKS

If the claim fees approved in the prior response have not yet been paid using Applicant's deposit account, then this paper serves as authorization to pay such claim fees as provided in the prior response.

Applicant's attorney thanks the Examiner for her kind telephone interview of November 9, 2005, and her reconsideration of this application. In this interview, the Sugizaki and Buynoski references were discussed, primarily with respect to claims 1 and 13. Applicant's attorney presented some of the basic points made in the remarks below.

Applicant is especially grateful of the Examiner's decision in this interview to withdraw the finality of the the outstanding rejection so as to permit Applicant to submit the foregoing claim amendments. Applicant understands from the interview that the Examiner only needs to do a final prior art search and, if no additional relevant reference is found in this search, the claims will otherwise be in condition for allowance.

**Applicant requests that the Examiner promptly send a notice of withdrawal of premature final rejection as described in the MPEP (reproduced below) as the remaining statutory six-month period for pendency of the application from the original Office Action mailing date is soon ending, and Applicant needs to docket the Examiner's withdrawal of final rejection from the telephone interview above.**

MPEP for Examiner's Reference:

### I. 706.07(d) Final Rejection, Withdrawal of, Premature

If, on request by applicant for reconsideration, the primary examiner finds the final rejection to have been premature, he or she should withdraw the finality of the rejection. The finality of the Office action must be withdrawn while the application is still pending. The examiner cannot vacate the final rejection once the application is abandoned.

Form paragraph **7.42** should be used when withdrawing the finality of the rejection of the last Office action.

**II. ¶ 7.42 Withdrawal of Finality of Last Office Action**

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

The amendments made by Applicant above are restated from the prior response faxed on October 18, 2005. According to MPEP 706.07(e), when a final rejection is withdrawn, all amendments filed after the final rejection are ordinarily entered. Applicant requests that all amendments above now be entered.

Applicant's remarks below are largely restated from the prior response.

In this response, claim 1 has been amended, claim 21 has been canceled without prejudice, and new claims 27-31 have been added. Thus, claims 1-14 and 22-31 are pending. The office action issued by the Examiner has been carefully considered by Applicant.

**Independent claim 1 has been rejected under 35 USC sec. 102(b) as being anticipated by Sugizaki (U.S. Patent No. 6,437,434).** Anticipation requires that every element of a claim be disclosed in a single prior art reference. Applicant's independent claim 1 has been amended to recite that the moat contains liquefied material (e.g., a polymer used to form a collar around a solder ball) that flows to the moat. The Examiner makes reference to a moat 7 of Sugizaki's Fig. 2B. Yet, Sugizaki, throughout its entire text, always only describes the outer moats 7 as being filled with elastomer. Also, Sugizaki's elastomer 10 is taught for coating bonding wires 9 (col. 5, lines 20-21) and is not taught or suggest for use in applying elastomer 10 to form around BGA ball 4. Thus, moat 7 is not able to contain liquefied material that flows to the moat where the liquefied

material is of a type provided to be formed around a solder ball on the solder ball pad, all as recited in Applicant's amended claim 1.

In particular, Figs. 3A to 3G are described by Sugizaki as illustrating the manufacture of the board 2 shown in Fig. 2B (see Sugizaki col. 4, lines 44-48, and col. 5, lines 22-23). Sugizaki describes that after openings are formed in the passivation layer 11, holes 8 and outer moats 7 are fill with elastomer 6 (see col. 4, lines 58-63). This is illustrated in Fig. 3D.

The Federal Circuit has stated that for a prior art reference to anticipate a claim, the reference must disclose each and every element of the claim with sufficient clarity to prove its existence in the prior art. Motorola, Inc. v. Interdigital Tech. Corp., 121 F.3d 1461, 43 USPQ2d 1481, 1490 (Fed. Cir. 1997). Further, in order to make a prima facie case of anticipation, as required by the Examiner, the prior art reference relied on must be interpreted in its entirety (and not based only on isolated portions of the reference) from the viewpoint of one of ordinary skill in the art. All of Sugizaki's moats are filled when using his described manufacturing processes for all embodiments, and one of ordinary skill in the art would not interpret Sugizaki to disclose a moat that is manufactured for containing a liquid.

Sugizaki uses the elastomer in moat 7 as part of the fundamental stress relief provided by Sugizaki's invention. Sugizaki describes the release of stress (col. 4, line 26) and that the elastomer layers 6 and 10 are "high-elastic" layers (col. 4, lines 15-16). Further, Sugizaki does not make mention of any liquefied material flow. Thus, Sugizaki does not recognize and is not presented with the problem of collection of any liquid flowing from the region of a solder ball or solder ball pad. One of ordinary skill in the art would not read the entirety of Sugizaki to disclose any moat built to contain a liquid.

**Independent claim 13 appears to have been rejected under 35 USC sec. 102(b) as being anticipated by or under 35 USC 103 as being obvious in view of Sugizaki**

**(U.S. Patent No. 6,437,434).** The Examiner's statutory basis for the rejection applying Sugizaki is not clearly stated. Applicant's claim 13 recites a polymer collar. However, Sugizaki does not disclose any polymer collar.

An obviousness rejection requires that there be some suggestion in the prior art to make a combination. The Examiner has stated that use of a polymer collar is admitted prior art, but has failed to provide any suggestion to combine such a collar with Sugizaki in a way that meets the limitations of Applicant's claim 13. Without such a suggestion, the burden has not been met to make a prima facie case of obviousness. Thus, there is no proper prima facie case of rejection of claim 13 under either 35 USC 102 or 103.

One of ordinary skill in the art would not be motivated to combine a polymer collar with the invention of Sugizaki due to the disadvantages that would result. First, if wire bond 9 (see, e.g., Sugizaki Fig. 2A) were applied prior to forming a polymer collar and solder ball drop, the printing of the polymer collar would likely damage the wirebond. Second, if the wirebond were applied after the polymer collar and solder ball drop, the wirebond pad adjacent to the solder ball would be covered in cured polymer collar material, thereby inhibiting wirebonding.

Moreover, note that Applicant's claim 14 recites that the moat prevents flow of liquefied polymer collar. As discussed above, nothing in Sugizaki teaches or suggests that moat 7 contain liquid. The Examiner's proposed combination would be a structure having a filled moat and a collar. This would not meet the limitations of Applicant's claim 14.

Applicant's new claim 27 recites a second passivation layer. In contrast, Sugizaki does not show a second passivation layer. It should be noted by the Examiner that Applicant's original dependent claim 8 also recites a second passivation layer.

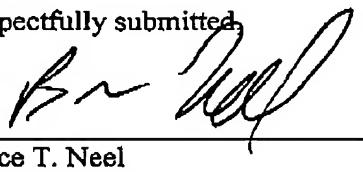
Applicant's new claim 28 recites a collar around the solder ball. Sugizaki does not itself disclose a collar as discussed above.

Applicant's new claim 29 recites that the moat is not formed in the semiconductor substrate. For example, Applicant's Fig. 4 shows the moat formed in a passivation layer 412, but not formed in semiconductor substrate 402. In contrast, Sugizaki's moat is formed in silicon interconnection board 2.

Applicant's other claims 2-12, 22-26 and 30-31 depend, directly or indirectly, from independent claims 1 and 13 and are believed allowable for at least the reasons discussed above.

In view of the above, Applicant respectfully requests reconsideration of this application and the allowance of all pending claims. It is respectfully submitted that the Examiner's rejections have been successfully traversed and that the application is now in order for allowance. Applicant believes that the Examiner's other arguments not discussed above are moot in light of the above arguments, but reserves the later right to address these arguments. Accordingly, reconsideration of the application and allowance thereof is courteously solicited.

Respectfully submitted,



Date: December 15, 2005

Bruce T. Neel
Reg. No. 37,406

Customer Number 33717
GREENBERG TRAURIG, LLP
2450 Colorado Avenue, Suite 400E
Santa Monica, CA 90404
Phone: (602) 445-8339
Fax: (602) 445-8100
E-mail: neelb@gtlaw.com

phx-fs1\1524454v02